Doc No. TT4-EA-10073

Revision. 2

# **Panasonic**

MOS FET

### MTM761230LBF

### MTM761230LBF

#### Silicon P-channel MOSFET

#### For Switching

#### ■ Features

• Low drain-source On-state Resistance : RDS(on) typ. = 36 m $\Omega$  (VGS = -4 V)

• Low drive voltage: 2.5 V drive

• Halogen-free / RoHS compliant

(EU RoHS / UL-94 V-0 / MSL : Level 1 compliant)

■ Marking Symbol :9C

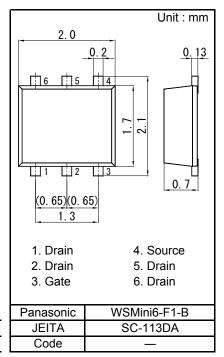
#### ■ Packaging

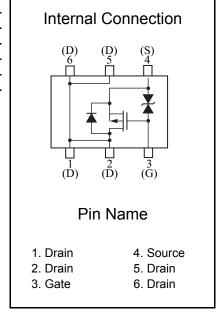
Embossed type (Thermo-compression sealing): 3 000 pcs / reel (standard)

■ Absolute Maximum Ratings Ta = 25 °C

Parameter	Symbol	Rating	Unit	
Drain to Source Voltage	VDS	-20	V	
Gate to Source Voltage	VGS	±10	V	
Drain Current	ID	-3	Α	
Drain Current (Pulsed) *1	IDp	-16	Α	
Total Power Dissipation *2	PD	700	mW	
Channel Temperature	Tch	150	°C	
Operating Ambient Temperature	Topr	-40 to +85	°C	
Storage Temperature Range	Tstg	-55 to +150	°C	

Note) \*1 Pulse width  $\leq$  10  $\mu$ s, Duty cycle  $\leq$  1 %





Established: 2007-11-07 Revised: 2013-06-18

<sup>\*2</sup> Measuring on ceramic board at 40 mm × 38 mm × 0.1 mm Absolute maximum rating PD Non-heat sink shall be made 150 mW.

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#### ■ Electrical Characteristics Ta = 25 °C ± 3 °C

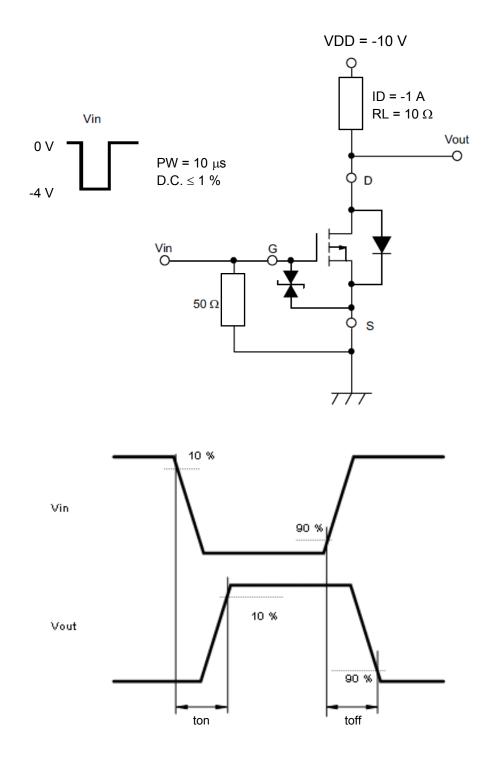
Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Drain-source Breakdown Voltage	VDSS	ID = -1 mA, VGS = 0 V	-20			V
Zero Gate Voltage Drain Current	IDSS	VDS = -20 V, VGS = 0 V			-1	μΑ
Gate-source Leakage Current	IGSS	$VGS = \pm 8 \text{ V}, VDS = 0 \text{ V}$			±10	μА
Gate-source Threshold Voltage	Vth	ID = -1 mA, VDS = -10 V	-0.4	-0.85	-1.3	V
Drain-source On-state Resistance *1	RDS(on)1	ID = -1 A, VGS = -4 V		36	55	mΩ
	RDS(on)2	ID = -0.5 A, VGS = -2.5 V		42	70	
Forward transfer admittance *1	Yfs	ID = -1 A, VDS = -10 V, f = 1 kHz	3.5			S
Input Capacitance	Ciss	VDS = -10 V, VGS = 0 V		1 000		pF
Output Capacitance	Coss	f = 1 MHz		100		
Reverse Transfer Capacitance	Crss	1 – 1 1011 12		100		
Turn-on Delay Time *2	ton	VDD = -10 V, VGS = 0 to -4 V		30		ns
		ID = -1 A		30		110
Turn-off Delay Time *2	toff	VDD = -10 V, VGS = -4 to 0 V		250	ns	ne
		ID = -1 A		230		115

Note) Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

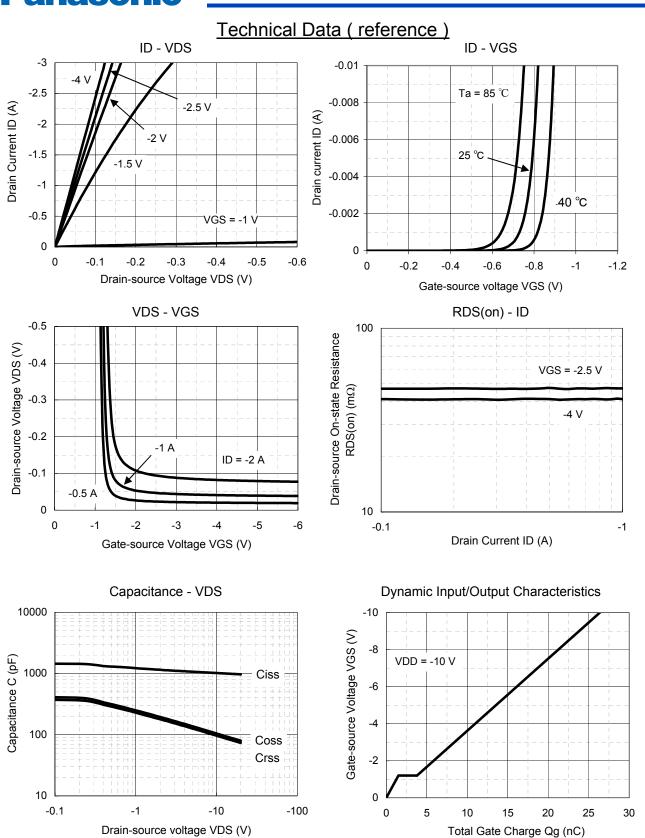
<sup>\*1</sup> Pulse test : Pulse width  $\leq$  300  $\mu$ s, Duty cycle  $\leq$  2 %

<sup>\*2</sup> Measurement circuit for Turn-on Delay Time / Turn-off Delay Time

\*2 Measurement circuit for Turn-on Delay Time / Turn-off Delay Time



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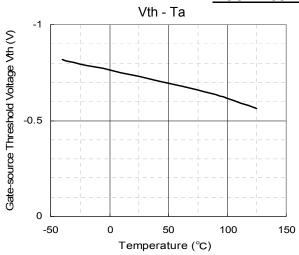


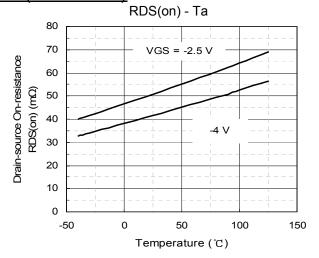
Established: 2007-11-07 Revised: 2013-06-18

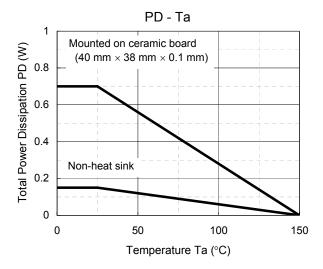
MOS FET

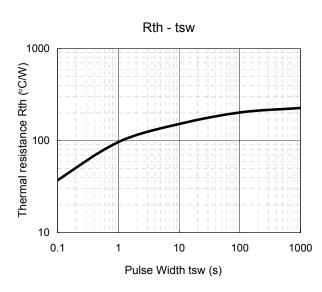
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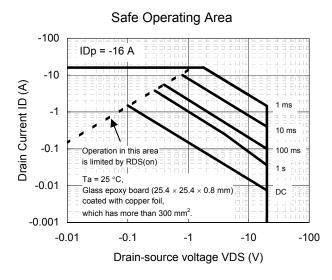
## Technical Data (reference)











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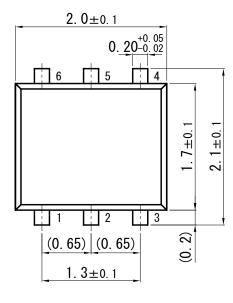
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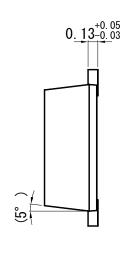
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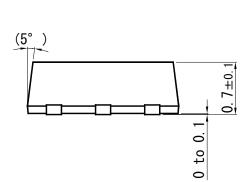
Unit: mm

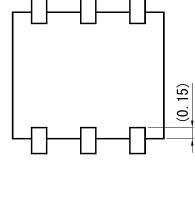
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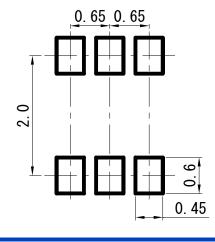








■ Land Pattern (Reference) (Unit : mm)



Established: 2007-11-07 Revised: 2013-06-18

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